REMARKS

Careful review and examination of the subject application are noted and appreciated.

COMPLETENESS OF THE OFFICE ACTION

Aside from a notice of allowance, Applicant's representative respectfully requests any further action on the merits be presented in a new Office Action. 37 CFR §1.104(b) states:

> (b) *Completeness of examiner's action.* The examiner's **action will be complete as to all matters**, except that in appropriate circumstances, such as misjoinder of invention, fundamental defects in the application, and the like, the action of the examiner may be limited to such matters of form need not be raised by the examiner until a claim is found allowable. (Emphasis added)

No arguments were presented for the rejections of claims 14-21. As such, the December 14, 2006 Office Action is incomplete and prosecution should continue.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments may be found in the specification, for example, on page 7 lines 15-21 and FIG. 1, as originally filed, and claims 6 and 7, prior to the instant amendment. Thus, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1-7 and 9-11 under 35 U.S.C. §103(a) as being unpatentable over Dorst '416 in view of Keskar et al. '989 (hereafter Keskar) has been obviated in part by appropriate amendment, is respectfully traversed in part, and should be withdrawn.

The rejection of claim 12 under 35 U.S.C. §103(a) as being unpatentable over Dorst and Keskar in further view of Ghaffari '932 has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 13-21 under 35 U.S.C. §103(a) as being unpatentable over Dorst, Keskar, and Ghaffari in further view of Tanaka et al, '376 (hereafter Tanaka) is respectfully traversed and should be withdrawn.

Dorst teaches an apparatus and methods for dedicated command port in memory controllers (Title). Keskar teaches a programmable memory controller (Title). Ghaffari teaches a method and apparatus for increasing the performance of communications between a host processor and a SATA or ATA device (Title). Tanaka teaches a processor capable of efficiently executing many asynchronous event tasks (Title).

Claim 1 provides both (i) a processor having **a first bus interface unit** to communicate on a system bus and (ii) an interface circuit having **a second bus interface unit** to communicate on the

system bus. In contrast, Keskar only shows a single bus interface unit 28 disposed between an execution unit 24 (alleged claimed processor) and an SDC 30 (alleged claimed interface circuit). Therefore, Dorst and Keskar, alone or in combination, do not appear to teach or suggest both (i) a processor having a first bus interface unit to communicate on a system bus and (ii) an interface circuit having a second bus interface unit to communicate on the system bus, as presently claimed.

Claim 1 further provides both (i) the processor configured to operate at a first data rate in response to **a first clock signal** and (ii) the interface circuit being configured to operate at a second data rate in response to **a second clock signal**. In contrast, both Keskar and Dorst appear to be silent regarding the two claimed clock signals. Furthermore, the rejection of claim 1 does not identify the alleged two clock signals in Keskar or Dorst. Therefore, Dorst and Keskar, alone or in combination, do not appear to teach or suggest both (i) the processor configured to operate at a first data rate in response to a first clock signal and (ii) the interface circuit being configured to operate at a second data rate in response to a second clock signal as presently claimed. Claims 10 and 11 provide language similar to claim 1. As such, the claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Claim 3 provides (from claim 1) that the interface circuit is configured to operate at the second data rate in response to the second clock signal and (from claim 3) the second clock signal is generated in response to the first clock signal. In contrast, FIG. 16A of Keskar shows that a clock signal m_clk (alleged claimed second clock signal) is only sent to an SDRAM and not used by the SDC 30 (alleged interface circuit). Therefore, Dorst and Keskar, alone or in combination, do not appear to teach or suggest that the interface circuit is configured to operate at the second data rate in response to the second clock signal and the second clock signal is generated in response to the first clock signal as presently claimed. As such, claim 3 is fully patentable over the cited references and the rejection should be withdrawn.

Regarding claim 13, the proposed motivation "providing this missing element" is an improper use of the claims as a template to combine the references. The only reason that a completion bit is "missing" from the proposed combination of Keskar, Dorst and Ghaffari is because the claim includes a completion bit. The Office cannot use what the Applicant has taught against the Applicant. Therefore, *prima facie* obviousness has not been established for the lack of proper motivation to modify/combine the references in accordance with MPEP 2143.01. As such, the rejection of claim 13 should be withdrawn.

Regarding claims 14-21, no arguments were presented for the rejection. Therefore, *prima facie* obviousness has not been established that the references teach or suggest all of the claimed elements. As such, the rejection of claims 14-21 should be withdrawn.

Claims 2-7, 9 and 12-21 depend from claim 1, which is now believed to be allowable. As such, the dependent claims are fully patentable over the cited references and the rejections should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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